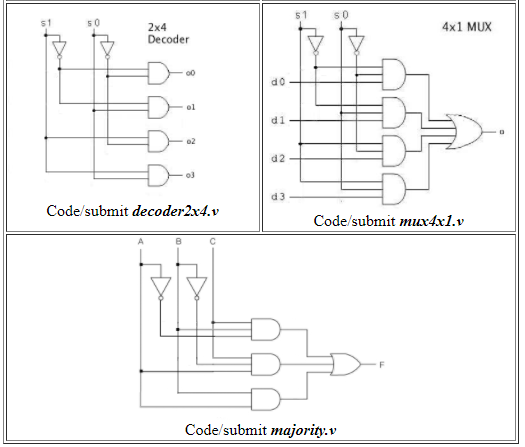
The diagrams below depicts different logic circuits that can be simulated with Verilog programs on the gate-logic level.



Reference : http://athena.csus.edu/~changw/205/prg/1/